



Features

- Frequency 106.25 MHz (or) 212.50 MHz
- Package 7X5 mm Ceramic
- RoHS Compliant Standard
- PECL Output
- Low Jitter
- Supply Voltage 3.3V

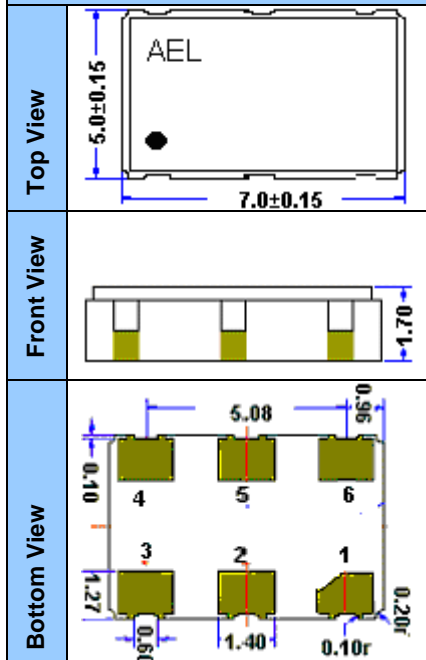
Table 1

Code	Stability Codes		F	G	M
	Frequency Stability		±20 PPM	±25 PPM	±50 PPM
E	Temperature Range	-10°C to +70°C			
I		-40°C to +85°C			

Denotes Available Denotes not Available

Mechanical Specification

Outline



All dimensions are in mm.
Black Dot indicates Pin No.1

Pin Configuration

Pin	Description
1.	Output Enable/Disable
2.	F Select (H-106.25, L-212.50)
3.	Ground
4.	Output
5.	Output*
6.	Supply

Parameters	Conditions	
Series:	XO 970	
Frequency:	106.25 MHz (or) 212.50 MHz	
Supply Voltage:	3.3 V±10%	
Output Waveform:	PECL	
Output High Level:	Min 2.275V (Referenced To Gnd) Vcc = 3.3V 0.975V (Referenced To Termination Voltage) -1.025V (Referenced To Vcc)	
Output Low Level:	Max 1.680V (Referenced To Ground) Vcc = 3.3V 0.380V (Referenced To Termination Voltage) -1.620V (Referenced To Vcc)	
Output Symmetry:	47% - 53% At 50% point of Vcc	
Jitter	0.9 pS RMS (max) 12KHz - 20MHz from output Frequency 2.0 pS RMS (max) 10 Hz – 1 MHz from output Frequency	
Rise / Fall time:	250 – 600 pS (Vth is 10% and 90% of waveform)	
Supply Current:	90mA (max)	
Enable/Disable Internal Pull-Up:	60Kohm (min) To Vcc	
Frequency stability:	(Table 1) Specify	
Temperature range:	(Table 1) Specify	
V Disable:	0.8Volts (max) Referenced to pad 3	
V Enable:	2.0Volts (min) Referenced to pad 3	
Output Leakage:	±50 uA pad1 low, device dsiald	
Enable Time:	10ns (max) Time for output to reach a logic state	
Disable Time:	10ns (max) Time for output to reach a high Zstate	
Start up time:	5ms (max) measure from the time, Vcc= 3.0 V	
Storage temperature range:	-55°C to +125° C	
Frequency Select Internal Pull – Up:	60 Kohm (min) To Vcc	Pad 2 Frequency Select Option For Dual Frequency
V Frequency select 212.50 MHz	0.8 V (max) Referenced To Gnd	
V Frequency select 106.25 MHz	2.0 V (min) Referenced To Gnd	

Specifications subject to change without notice
Revision No. 12b of May 2008

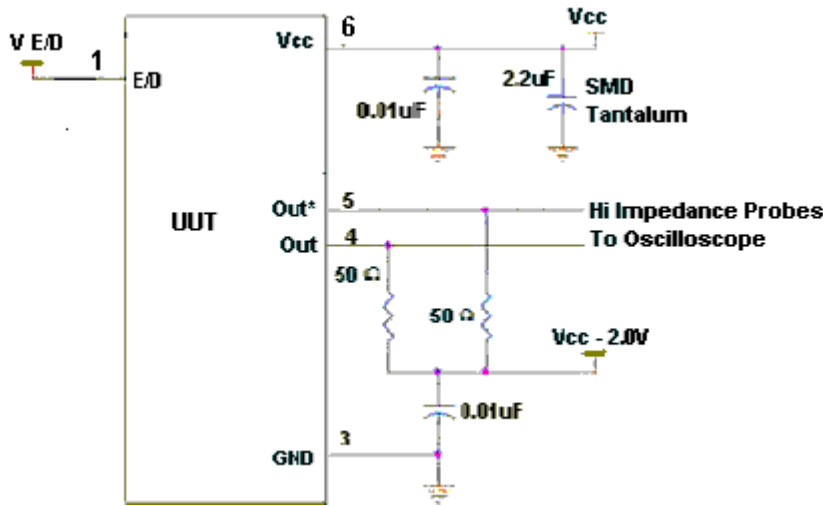
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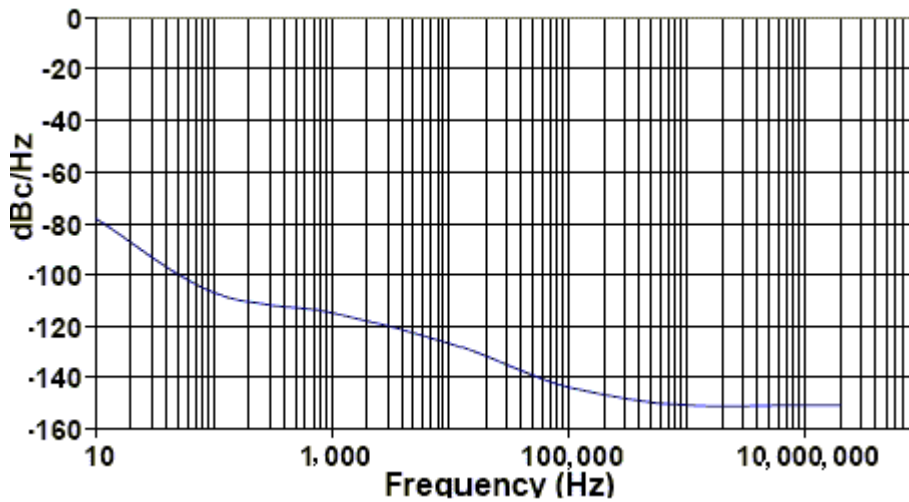
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LOAD CIRCUIT

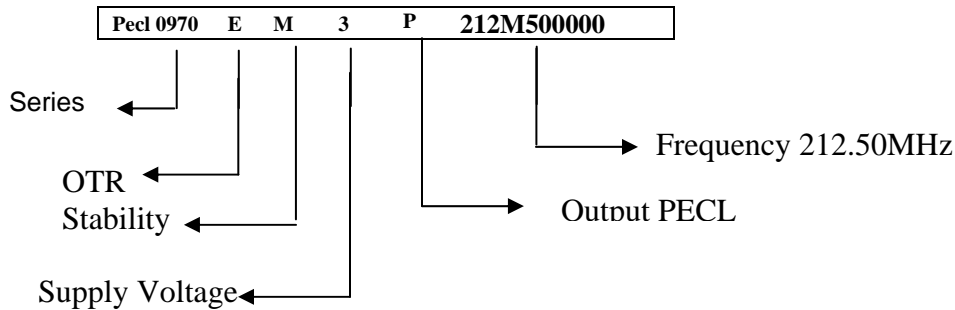


Typical Phase-Noise Response



Ordering Information

Example



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