XO 980

Features

- Frequency Range 10.9 – 766 MHz
  876 – 1,175 MHz
- Package 7X5 mm Ceramic
- PECL Output
- RoHS Compliant Standard
- Low Jitter

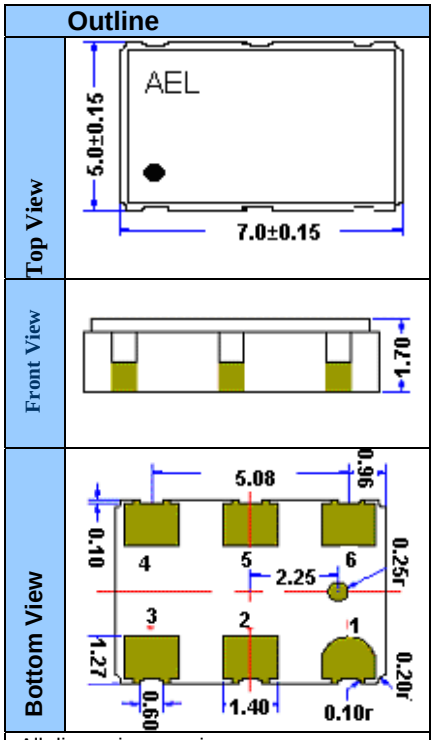
Table 1

Code	Stability Codes / Frequency Stability		F ±20 PPM	G ±25 PPM	M ±50 PPM
E	Temperature Range	-10°C - +70°C			
I	Temperature Range	-40°C - +85°C			

Denotes Available Denotes not Available

Mechanical Specification

Outline



All dimensions are in mm.

Pin Configuration

PIN	Description
1	No Connect
2	Output Enable/Disable
3	Ground
4	Output
5	Output*
6	Supply

Parameters	Conditions	
Series:	XO 980	
Frequency Range:	10.9 - 766 MHz 876 – 1,175 MHz	
Supply Voltage:	3.3V ± 10%, 2.5V ± 10%	
Output Waveform:	PECL	
Output High Level:	Min	Max
	2.12V 0.82V -1.18V	2.49V (Referenced To Ground) 1.19V (Referenced To TerminationVoltage) -0.81V (Referenced to Vcc)
Output Low Level:	Min	Max
	1.83V 0.53V -1.47V	1.99V (Referenced To Ground) 0.69V (Referenced To TerminationVoltage) -1.31V (Referenced To Vcc)
Output Symmetry:	47% - 53% At 50% point of Vcc	
Jitter	0.6 pS RMS (max) 12KHz - 20MHz from output frequency 2.8 pS RMS (max) 10 Hz - 20MHz from output frequency	
Rise / Fall time:	100 – 300 pS (Vth is20% and 80% of waveform)	
Supply Current:	90mA (max)	
Enable/Disable Internal Pull-Up:	50Kohm (min) To Vcc	
Frequency stability:	(Table 1) Specify	
Temperature range:	(Table 1) Specify	
V Disable:	0.8Volts (max) Referenced to pad 3	
V Enable:	2.0Volts (min) Referenced to pad 3	
Output Leakage:	±50 uA (Vout = Vcc) ±50 uA (Vout = 0V)	
Enable Time:	10ns (max) Time for output to reach a logic state	
Disable Time:	10ns (max) Time for output to reach a high Zstate	
Start up time:	5ms (max) Time for output to reach specified frequency	
Storage Temperature Range:	-55°C to +125° C	

Specifications subject to change without notice
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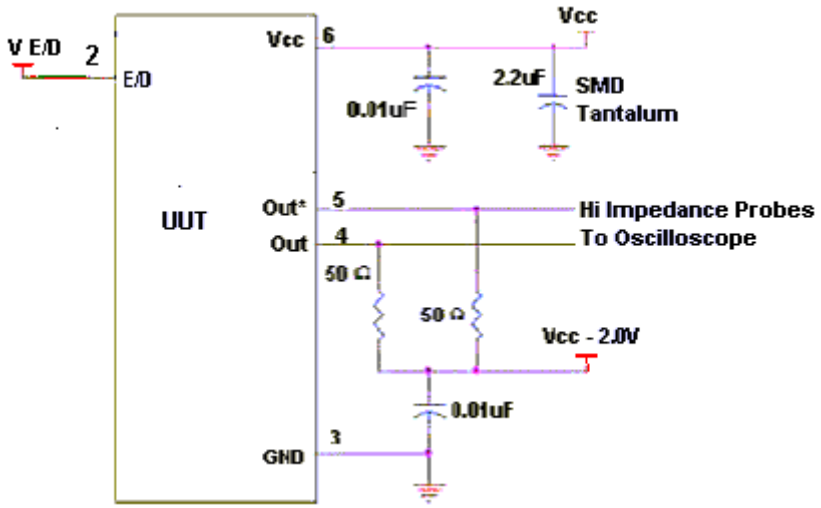
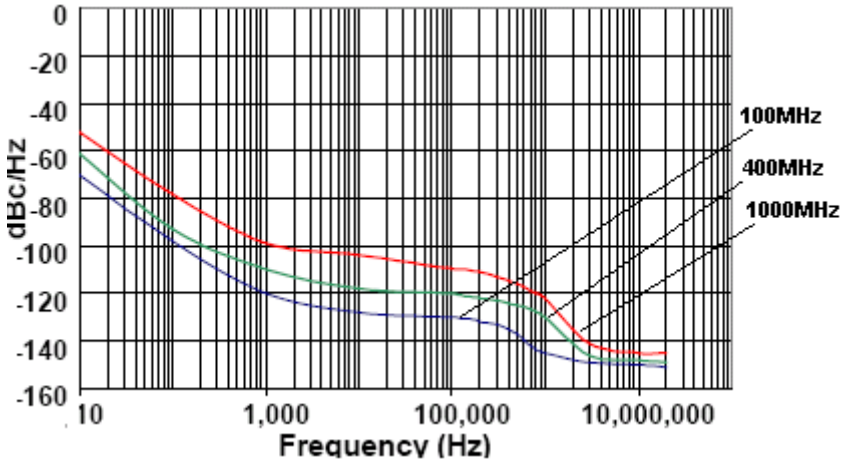
LOAD CIRCUIT



Typical Phase-Noise Response



Ordering Information

Example

Pecl 0980	E	M	3	P	766M000000

Series

OTR

Stability

Supply Voltage

Output PECL

Frequency 766MHz

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